Claim Rejections Under 35 USC §102

I. Claims Rejected Under 35 U.S.C §102(e) As Being Anticipated By Lin

Claims 1-2 and 8-19 stand rejected under 35 U.S.C §102(e) as being anticipated by Lin (U.S. Patent No. 6,631,452) ("Lin"). Applicants respectfully traverse this rejection and submit that Lin fails to disclose each and every limitation recited in claims 1-2 and 8-19.

A. Independent Claims 1 and 8 Patentably Distinguished over Lin

Independent claims 1 and 8 are directed towards a microprocessor that contains a mechanism for detecting an *imminent* register window overflow or underflow condition and *generating an instruction* to *avoid a trap* from the register window overflow or underflow condition. That is, the detector of the microprocessor detects that a register window overflow or underflow condition will occur prior to the occurrence of a trap responsive to the overflow or underflow condition. In response to this detection, the generator of the microprocessor generates an instruction to manipulate microprocessor storage to avoid the occurrence of the trap. In this manner, the microprocessor does not execute the trap responsive to the register window overflow or underflow condition.

Lin does not disclose a mechanism for detecting an *imminent* register window overflow or underflow condition and *generating an instruction* to *avoid a trap* from the register window overflow or underflow condition. In contrast to the claimed invention, Lin detects the occurrence of a register window overflow or underflow condition as it occurs. In Lin, the Examiner cites the state machine of the microprocessor's register stack engine ("RSE") as a detector of register window overflow and underflow conditions (Lin, column 8, lines 49 to column 9, line 5; Figure 6). The state machine checks the processor for a currently pending

instruction and then executes the instruction (Lin, column 8, lines 41-43, column 9, lines 1-3). If executing the instruction triggers an overflow or underflow condition, the RSE executes either a mandatory spill or fill operation. At the time the state machine detects the overflow or underflow condition, it is mandatory to execute the spill or fill operation. As such, the state machine detects the overflow or underflow condition as it occurs. In contrast, the claimed invention detects an *imminent* underflow or overflow condition prior to the mandatory execution of the spill or fill operation. Therefore, Lin fails to disclose a mechanism for detecting an *imminent* register window overflow or underflow condition.

Moreover, Lin does not *avoid the trap* that occurs in response to a register window overflow or underflow condition. When the RSE detects a mandatory fill or spill operation, it stalls the processor to execute the fill or spill operation (Lin, column 8, lines 61-64). This is the costly trap triggered by a fill or spill operation that the claimed invention avoids. Although Lin may try to reduce the occurrence of mandatory fill or spill operations, these mandatory operations still occur in Lin. When these operations occur, Lin will trigger traps and stall processor execution (Lin, column 10, lines 58-60). In contrast, the claimed invention *avoids a trap* responsive to the register window overflow or underflow condition.

Furthermore, Lin does not *generate an instruction* to *avoid the trap.* As discussed above, Lin does not *avoid the trap* from register window overflow or underflow conditions. Additionally, Lin does not *generate an instruction* when it detects a register window overflow or underflow condition. When the RSE of Lin detects a mandatory fill or spill operation, it executes an already existing procedure of either a RSE load or RSE store (Lin, column 7, lines 45-58) to transfer data to and from the backing store (Lin, column 3, lines 47-67). As such, Lin

is not *generating an instruction* but executing an existing procedure. In contrast, the claimed invention *generates an instruction* to *avoid the trap.*

For the aforementioned reasons, Lin fails to disclose a mechanism for detecting an *imminent* register window overflow or underflow condition and *generating an instruction* to *avoid a trap* from the register window overflow or underflow condition. Therefore, Applicants submit that claims 1, 8 and 16 are patentable and in condition for allowance. Accordingly, Applicants request the Examiner to withdraw the rejection of claims 1 and 14 under 35 U.S.C §102.

B. Independent Claim 16 Patentably Distinguished over Lin

Independent claim 16 is directed to a method in a microprocessor to determine an *imminent* register window spill or fill and manipulate the storage of register window contents to *avoid a trap* from the register window spill or fill. That is, the method determines that a register window spill or fill will occur prior to the occurrence of a trap responsive to the register window spill or fill. In response to this determination, the method manipulates the contents of register windows in storage to avoid the occurrence of the trap. By this method, the microprocessor does not execute the trap responsive to the register window spill or fill.

Lin does not disclose a method for determining that a register window spill or fill is *imminent*. As discussed above, Lin determines the occurrence of a register window spill or fill and executes the mandatory spill or fill operation as the register window spill or fill occurs (Lin, column 8, lines 41-43 and column 9, lines 1-3). In contrast, the claimed invention determines an *imminent* register window spill or fill prior to the mandatory execution of the spill or fill operation. Therefore, Lin fails to disclose determining an *imminent* register window spill or fill.

Moreover, Lin does not *avoid the trap* that occurs in response to a register window spill or fill. As discussed above, when a mandatory fill or spill condition is detected, the method of Lin triggers traps and stalls the processor in executing the mandatory fill or spill operation (Lin, column 10, lines 58-60). In contrast, the method of the claimed invention *avoids a trap* responsive to the register window spill or fill.

For the aforementioned reasons, Lin fails to disclose a method in a microprocessor to determine an *imminent* register window spill or fill and manipulate the storage of register window contents to *avoid a trap* from the register window spill or fill. Therefore, Applicants submit that claim 16 is patentable and in condition for allowance. Accordingly, Applicants request the Examiner to withdraw the rejection of claim 16 under 35 U.S.C §102.

C. Claims Dependent from Patentable Independent Claims 1, 14 and 16

Claims 2, 8-13, 15 and 17-19 depend on independent claims 1, 14 and 16, respectively, which are patentably distinguished over Lin for the above-discussed reasons. Claims 2 and 8-13 depend on independent claim 1, and, thus, incorporate all the patentable limitations of claim 1. Claim 15 depends on independent claim 14, and, thus, incorporates all the patentable limitations of claim 14. Claims 17-19 depend on independent claim 16, and, thus, incorporate all the patentable limitations of claim 16. As such, Lin does not anticipate claims 2, 8-13, 15 and 17-19. Therefore, Applicants submit that claims 2, 8-13, 15 and 17-19 are patentable and in condition for allowance. Accordingly, Applicants request the Examiner to withdraw the rejection of claims 2, 6-7, 15 and 17-19 under 35 U.S.C §102.

Claim Rejections Under 35 USC §103

II. Claims Rejected Under 35 U.S.C §103 As Unpatentable Over Lin

Dependent claims 3-7 are rejected under 35 U.S.C §103(a) as being unpatentable over Lin. Applicants respectfully traverse this rejection and contend that Lin fails to detract from the patentability of claims 3-7.

A. Non-obviousness of Claims Dependent from Patentable Independent Claim 1

Lin fails to teach or suggest each and every claim limitation of dependent claims 3-7. Claims 3-7 depend on independent claim 1, and, thus, incorporate all the patentable limitations of claim 1. Independent claim 1 is directed towards a microprocessor that contains a mechanism for detecting an *imminent* register window overflow or underflow condition and *generating an instruction* to *avoid a trap* from the register window overflow or underflow condition.

Lin does not teach or suggest a mechanism for detecting an *imminent* register window overflow or underflow condition and *generating an instruction* to *avoid a trap* from the register window overflow or underflow condition. Lin seeks to perform speculative fill and spill operations when processor bandwidth is available. For mandatory fill and spill operations, Lin does not seek to avoid the trap that occurs in performing the mandatory fill and spill operations. Lin is directed towards executing the mandatory fill or spill operation in due course, which causes a trap and stalls the processor as required. Furthermore, Lin does not teach or suggest generating an instruction to avoid the trap of the mandatory operation. Rather, Lin focuses on using existing load and store procedures. As such, Lin does not teach or suggest detecting an *imminent* spill or fill operation and *generating an instruction* to *avoid a trap* from the spill or fill operation.

For the aforementioned reasons, Applicants submit that Lin does not detract from the patentability of claim 1. As such, dependent claims 3-7 are patentable and in condition for allowance. Therefore, Applicants respectfully request the withdrawal of the Examiner's rejection of claims 3-7 under 35 U.S.C. §103.

B. Non-obviousness of Dependent Claims 3-7

In addition to the patentable limitations of independent claim 1, dependent claims 3-7 are directed towards a microprocessor further comprising a cache for caching instructions for introduction into an execution stage and wherein the microprocessor's detector examines the instructions in the cache to determine if a register window overflow or underflow condition is imminent. In the Office action, the Examiner admits that Lin does not teach the limitations recited in these dependent claims. In the rejection of these dependent claims, the Examiner cites Lin to suggest one ordinarily skilled in the art might modify Lin to look further up the instruction path into the instruction cache to see what instructions are coming up. Applicants contend that one ordinarily skilled in the art at the time invention was made would not find a motivation or suggestion in Lin to modify Lin as the Examiner suggests.

In the Office action, the Examiner equates the state machine of the RSE in Lin to the detector of the claimed invention. As a state machine, it is not prospective in nature. The state machine monitors the processor for currently pending instructions (Lin, column 8, 58-60), and maintains the current state of the register stack based on the currently pending instruction. The monitor (610, Fig. 6) of the state machine detects from the processor if there is currently a register instruction to execute. If so, it executes the register instruction and moves to the state adjust state (620, Fig. 6). If the state indicates a mandatory fill or spill operation from the

register instruction, the state machine executes the mandatory spill or fill operation. Then, the state machine transitions back to the monitor state (610, Fig 6) to monitor and detect the next pending register instruction, if any. If there is not a pending instruction, then the state machine checks for availability of memory channel bandwidth to perform storage operations. As such, the state machine is focused on the current state of the register stack engine and the currently pending instruction of the processor, if any. The state machine does not look further up the instruction path for future instructions. As such, Lin does not teach or suggest looking at future instructions. Therefore, one ordinarily skilled in the art would not find a motivation or suggestion in Lin to modify the state engine of Lin to look further up the instruction path for future instructions.

For the aforementioned reasons, Applicants submit that Lin does not detract from the patentability of claims 3-7. Accordingly, Applicants respectfully request the withdrawal of the Examiner's rejection of claims 3-7 under 35 U.S.C. §103.